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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,998	02/04/2004	Vincent Nguyen	200315049-1	4074

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EXAMINER	
LE, DIEU-MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n N .	Applicant(s)	
	10/771,998	NGUYEN ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4&4/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This Office Action is in response to the application 10/771,998 filed on 06/14/06.

2. Claims 1-27 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dell et al. (U.S. 6,092,146 hereafter referred to as Dell) in view of Huang et al. (U.S. 5,008,885 hereafter referred to as Huang).

As per claim 1:

Dell substantially teaches the invention. Dell teaches:

- A memory module [abstract, fig.1-5, col. 1, lines 65 through col. 2, lines 20]; comprising:

- A plurality of memory circuits, wherein at least one of the memory circuits comprising a serial presence detect (SPD) memory circuit [fig.1-5, abstract, col. 1, lines 65 through col. 2, lines 20; col. 4, lines 34 through col. 5, lines 19];
- testing logic coupled to at least one of the plurality of data lines [fig.1-5, col. 3, lines 45-50].

Dell does not explicitly address:
- inject a memory error into data lines.

However, Dell does disclose capability of:
- A dynamically configurable memory for computer system [abstract, fig.1-5, col. 1, lines 5-10] comprising:
- a connectivity among memory modules, I2C bus controller, memory controller, serial presence detects (SPDs), ect… [fig. 1-5 , col. 3, lines 28-50].
- ***SIMMs memory error insertion, detection, and correction means used to test memory modules*** [fig. 5, col. 4, lines 55 through col. 5, lines 19].

In addition, Huang explicitly teaches:

- A computer testing system having error injection, detection, and data recovery capabilities [abstract, fig. 1, col. 1, lines 5-10] comprising:

- ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** [col. 1, lines 44 through col. 2, lines 22].

Therefore it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Dell's ***SIMMs memory error insertion, detection, and correction means used to test memory modules*** as being the inject a memory error into data lines as claimed by Applicant. This is because Dell explicitly performed memory testing via error detection and correction functionality from memory insertion feature in supporting the memory/data storing, testing, evaluating, and processing. By utilizing these capabilities, the data between the data storage device or memory module and information data communication system (i.e., host/servers/gateways/switches environment/SPD) can be directed or redirected promptly and functioned properly

during error insertion or injection process in supporting the computer memory operation; second, by applying the ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** as taught by Huang in conjunction with the dynamically configurable memory for computer system as taught by Dell, the computer data memory module including row/column data lines capabilities can enhance its memory operation performance, more specifically to ensuring the best testing logic/procedure applied along with its error detected, corrected routing addresses and protocol in the storage area.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory operation availability and network/system performance therein with a mechanism to enhance the data processing, connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2 and 4:

Dell further teaches:

- the testing logic, the memory module, and the SPD memory circuit are coupled to a communication bus [fig. 3, col. 3, lines 1-14 and lines 28-50];
- a bus controller that transfers data from the SPD memory circuit [fig. 3, col. 3, lines 1-14 and lines 28-50].

In addition, Huang explicitly teaches:
- A computer testing system having error injection, detection, and data recovery capabilities [abstract, fig. 1, col. 1, lines 5-10] comprising:
- ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** [col. 1, lines 44 through col. 2, lines 22].

As per claims 3 and 5:

Dell further teaches:
- a connectivity among memory modules, I2C bus controller, memory controller, serial presence detects (SPDs), ect… [fig. 1-5 , col. 3, lines 28-50].

- testing logic coupled to at least one of the plurality of data lines [fig.1-5, col. 3, lines 45-50].

Dell does not explicitly address:

- a counter of the number of data lines to electrically bias (voltage).

However, Dell does disclose capability of:

- A dynamically configurable memory for computer system [abstract, fig.1-5, col. 1, lines 5-10] comprising:

- ***SIMMs memory error insertion, detection, and correction means used to test memory modules utilizing memory row/column data input/output via its operation voltages*** [col. 5, lines 56 through col. 6, lines 15].

In addition, Huang explicitly teaches:

- A computer testing system having error injection, detection, and data recovery capabilities [abstract, fig. 1, col. 1, lines 5-10] comprising:

- ***error injection means used for testing and evaluating machine via its counter machine (i.e.,***

processing machine, memory module, programmable devices, etc…) ***states*** [col. 1, lines 44 through col. 2, lines 22].

Therefore it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to realize that the combination of Dell's ***SIMMs memory error insertion, detection, and correction means used to test memory modules utilizing memory row/column data input/output via its operation voltages*** and Huang's ***error injection means used for testing and evaluating machine*** via ***its counter machine*** (i.e., processing machine, memory module, programmable devices, etc…) ***states*** do teach applicant's counter of the number of data lines to electrically bias (voltage) limitation. This is because both Dell and Huang explicitly demonstrated memory testing via error detection/correction and injection functionality in supporting the memory/data storing, testing, evaluating, and processing. It is further obvious because Dell illustrated the data memory including row and column testing via its proper operation voltage arrangements [col. 6, lines 9-11]. By utilizing these capabilities, the computer data memory module including row/column data lines

capabilities can enhance its memory operation performance, reliability, and maximizing its throughput.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory operation availability and network/system performance therein with a mechanism to enhance the data processing, and connectivity.

As per claims 6-7:

Dell further teaches:

- the testing logic utilizes fig.1-5, col. 3, lines 45-50:

    -- a column access strobe (CAS) latency stored in the SPD memory circuit [fig 4, col. 3, lines 50-65 and col. 5, lines 42-55];

    -- a memory rank stored in the SPD memory circuit [col. 4, lines 34 through col. 5, lines 48];

Dell does not explicitly address:

- inject a memory error into data lines.

However, Dell does disclose capability of:

- A dynamically configurable memory for computer system [abstract, fig.1-5, col. 1, lines 5-10] comprising:

- a connectivity among memory modules, I2C bus controller, memory controller, serial presence detects (SPDs), ect… [fig. 1-5 , col. 3, lines 28-50].

- ***SIMMs memory error insertion, detection, and correction means used to test memory modules*** [fig. 5, col. 4, lines 55 through col. 5, lines 19].

In addition, Huang explicitly teaches:

- A computer testing system having error injection, detection, and data recovery capabilities [abstract, fig. 1, col. 1, lines 5-10] comprising:

- ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** [col. 1, lines 44 through col. 2, lines 22].

Therefore it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Dell's ***SIMMs memory error insertion, detection, and correction means used to test***

memory modules as being the inject a memory error into data lines as claimed by Applicant. This is because Dell explicitly performed memory testing via error detection and correction functionality from memory insertion feature in supporting the memory/data storing, testing, evaluating, and processing. By utilizing these capabilities, the data between the data storage device or memory module and information data communication system (i.e., host/servers/gateways/switches environment/SPD) can be directed or redirected promptly and functioned properly during error insertion or injection process in supporting the computer memory operation; second, by applying the ***error injection means used for testing and evaluating machine (i.e., processing machine, memory module, programmable devices, etc…)*** as taught by Huang in conjunction with the dynamically configurable memory for computer system as taught by Dell, the computer data memory module including row/column data lines capabilities can enhance its memory operation performance for the same reasons set forth as described in claim 1, **supra**.

As per claims 8-15:

Due to the similarity of claims 8-15 to claims 1-7 except for a method comprising memory module, data communication, testing logic, etc… instead of a memory module comprising memory circuit, data transferring, testing logic via applied a bias voltage, etc….; therefore, these claims are also rejected under the same rationale applied against claims 1-7. **In addition, all of the limitations have been noted in the rejection as per claims 1-7. Such as *an inter-integrated circuit (I2C) communication bus* as disclosed by Dell [fig. 3, col. 3, lines 2-3].**

As per claims 16-20:

These claims are the same as per claims 1-7. The only minor different is that these claims are directed to a **computer-readable media storing instructions executables by a computer system** instead of the memory module comprising plurality of memory circuits, a serial presence detect (SPD), test logic, etc… as described in claims 1-7. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that a **computer-readable media** is a necessary item for such data memory networking system, more specifically,

memory module with test logic. Since the memory data testing system obviously needs a means for instruction or code means resided within the **computer-readable media** for performing the data storing, receiving, transmitting, operation via the inject memory error testing capability. Therefore, these claims are also rejected under the same rationale applied against claims 1-7. **Such as *an inter-integrated circuit (I2C) communication bus* as disclosed by Dell [fig. 3, col. 3, lines 2-3].**

As per claims 21-27:

Due to the similarity of claims 21-27 to claims 1-7 except for a system comprising ***MEANS*** for storing data, ***MEANS*** for transferring data, ***MEANS*** for applying a bias voltage, etc… instead of a memory module comprising memory circuit, data transferring, testing logic via applied a bias voltage, etc….; therefore, these claims are also rejected under the same rationale applied against claims 1-7. **In addition, all of the limitations have been noted in the rejection as per claims 1-7.**

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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7/15/06